Building an Open Chiplet Economy

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Collocated with HPCA 2023 Montreal Canada

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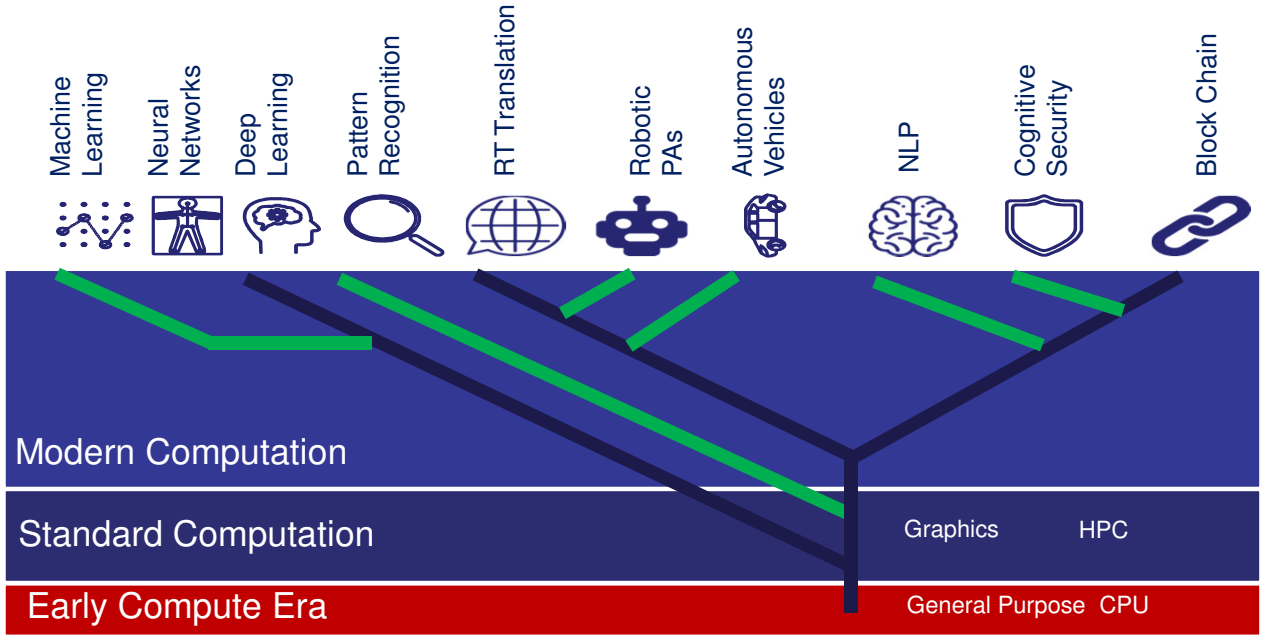
Open Compute Project Foundation

Community-driven hyperscale innovation for all.

The Rise of Diverse Domain-Specific Architectures



AI and Machine-learning and data-heavy workloads have exploded in past 5 years and will diversify as new applications are discovered constantly…

From D Jani, Meta, Sep 19

Chiplets Will be Everywhere Chips Are

Semiconductor worldwide revenue by end vertical, sales (source: Gartner)

End vertical	Example	2020	Power	I/O	Other
Automotive	ADAS, Infotainment Chassis	8.3%	10s of W	10s of Gbps	Long life
Communication	Smartphones	32.9%	< 10 W	Gbps	Rapid churn
Consumer	TVs, Digital Set-Top Box	10.4%	< 10 W	Gbps	Cost sensitive
Data processing	PCs, Servers, Storage Media	37.7%	100s of W	100s of Gbps	Rapid churn
Industrial	Automation, Healthcare, Security	10.7%	10s of W	10s of Gbps	Harsh environment

Diversity in power, performance, cost, business requirements.

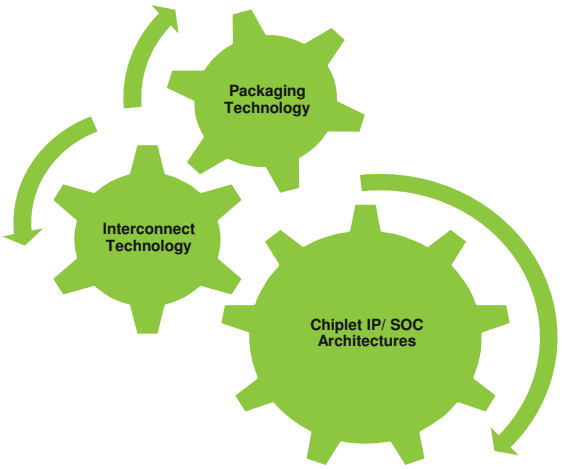
Accenture: Harnessing the Power of the Semiconductor Value Chain

For a Chiplet Economy…

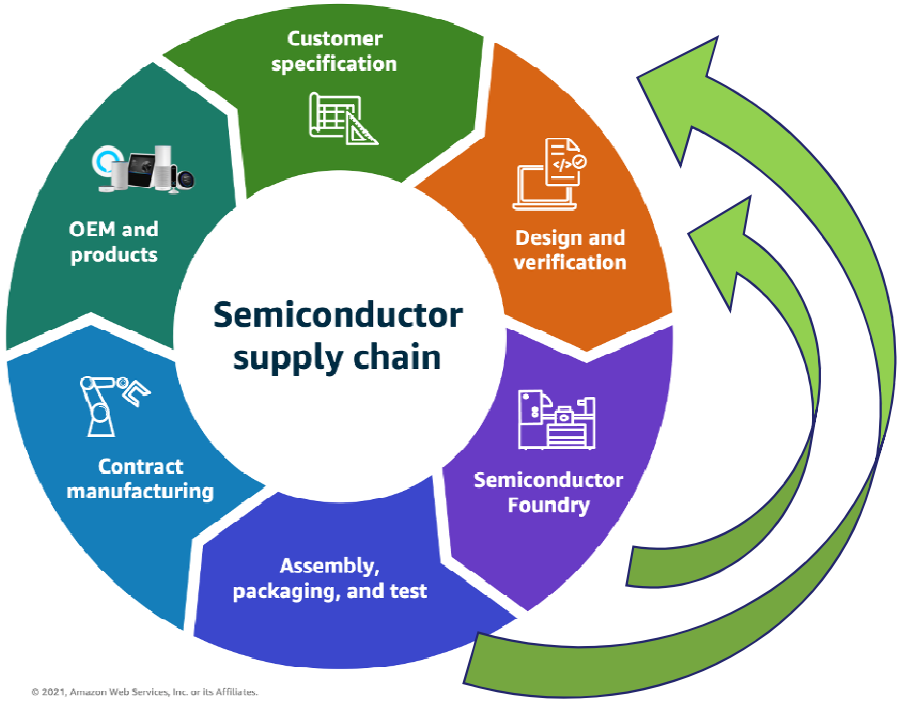
To meet huge diversity in requirements we need

- **A core set of application specific standards**
- **A low barrier to entry for innovation**
- **Freely customizable for applications**

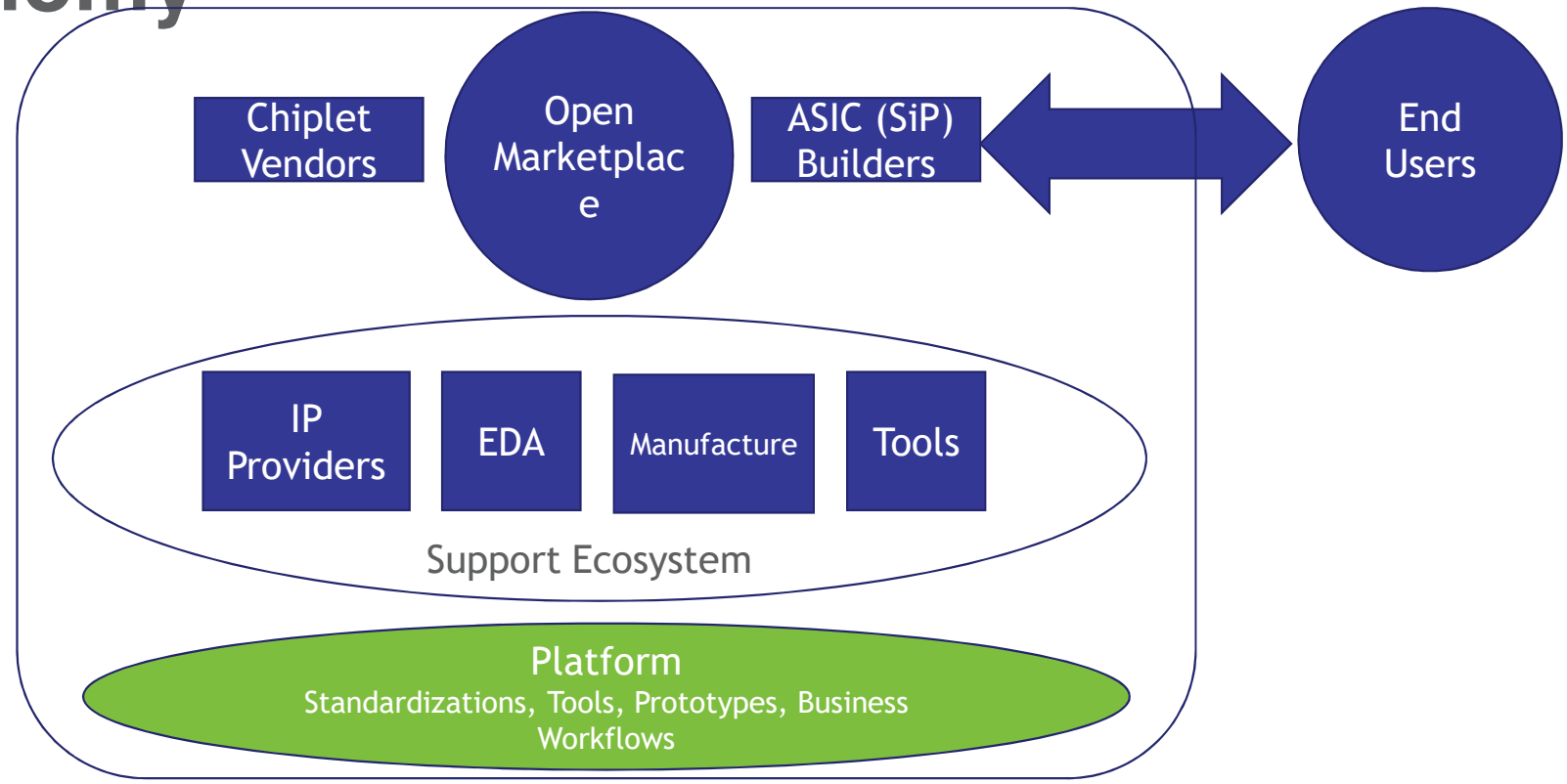
Build and let the market use as it sees fit



…Need New Integration Across The Value Chain



Establishing a New Open Chiplet Economy

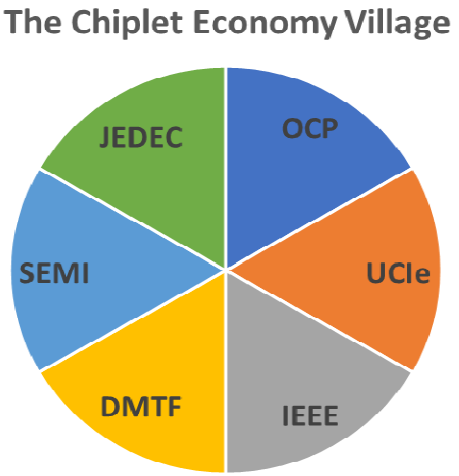


Platform Elements for Rapid Growth

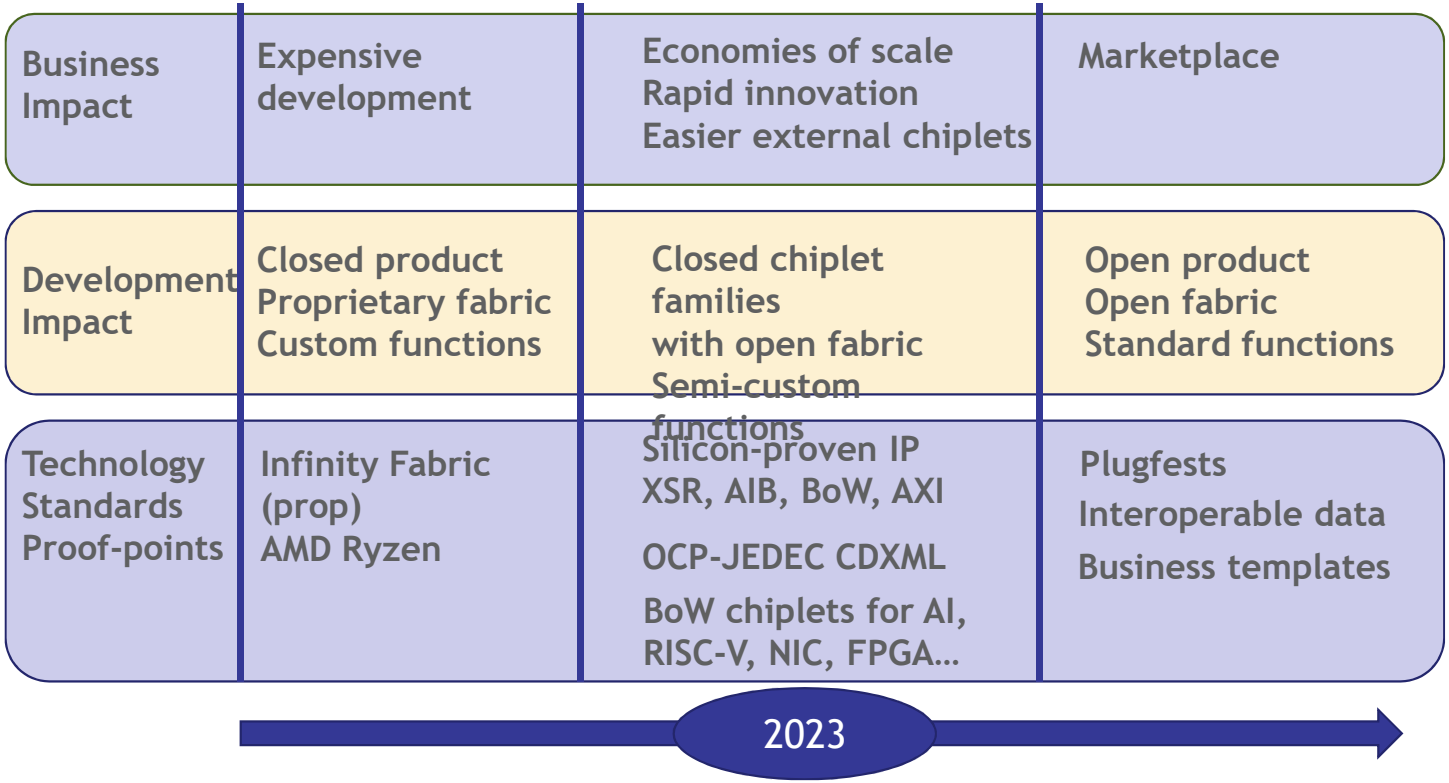
	Business Workflow	SiP Integration	SiP Design	Chiplet Interconnect
Standards		Digital Chiplet Physical Descriptions Modularity	Digital Chiplet Functional Descriptions	PHY layer Link layer Trans. layer
Tools and Reference	SiP cost models Known-Good Die contracts	Package Analysis & Tools Device Test	Architecture Exploration Test Package	Selection Guides Channel models Open Designs
Production Support	Business Logistics	In-field management	Chiplet Catalog	

It Will take a Village…

- JEDEC: Microelectronic Industry Standards
- OCP: Modularity and DC Requirements
- UCIe: Chiplet Interconnect & Market Development
- IEEE HIR: Packaging & Assembly Roadmaps
- DMTF: Device Management
- SEMI: Business Models



…And It is a journey that has already started

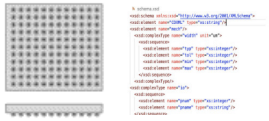


OCP Investing to Establish an Open Chiplet Economy

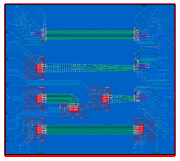
(Accelerating advanced computing)

Open Domain Specific Architecture Project, Since 2018

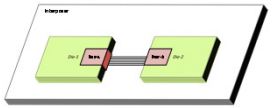
Business Workflows



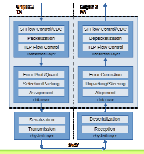
Chiplet Description Schema



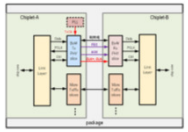
Chiplet Test Bench



Interconnect Comparison Benchmark



Logical Interconnects



Physical Interconnects

Thermal Management for SiP

Co-packaged Optics

In-package Health Monitoring

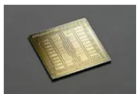
OCP ODSA Key Achievements to date

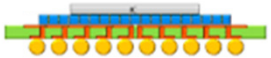
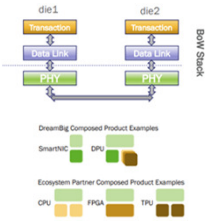
- Reference tools
  - D2D comparison spreadsheet
  - Chiplet cost model
  - Channel models
- OCP-JEDEC CDXML part models
  - Standard for chiplet physicals description
- No-license cost BoW spec from many vendors
  - Scalable 65nm-7nm, Laminate/advanced packaging, stable gen 2 draft
  - Silicon-proven, measured < 0.5 pJ/bit, 800 Gbps/mm in laminate packaging
- Open-source package design
  - First open cross-company D2D interop demo

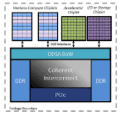
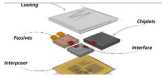
https://www.opencompute.org/wiki/Server/ODSA

ODSA Impact is Significant and Continues to Grow

- Blue Cheetah family of BoW-based D2D solutions
- eTopus/Quicklogic/Comira - BoW/FPGA/Ethernet I/O
- NXP BoW256 PHY development
- BoW PHY Interoperability Testing
- DreamBig BoW based Chiplet Platform for SmartNIC's
- D-Matrix BoW D2D Interface for Multi-Chiplet AI System
- Ventana Micro Systems RISC-V CPU using BoW
- Fraunhofer implements BoW on Samsung 5nm Technology

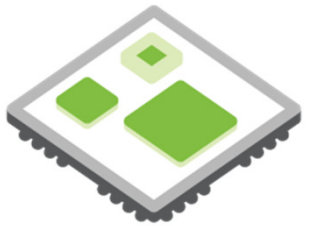


Takeaways

- Market is diverse, there will be many domain-specific solutions
- Rapid innovation requires light standards with
  low barriers to entry, reuse and adaptation
- Open communities are critical to accelerating the Open Chiplet Economy



Please Join Us

Join

- Project Mailing Lists
- Project Calls

Drive

- Project Focus
- Thought Leadership

Run

- Project Leaders
- Technical Steering Committee

Contribute

- Specifications
- Products & Facilities

Attend

- OCP Summits
- 3rd Party events
- OCP Panels
- OCP Engineering Workshops
- OCP Webinars
- OCP Events

Learn more at opencompute.org!

Community-driven hyperscale innovation for all.

Need Standardized Business Workflows & Relationships

Responsibility for Quality

- Economic model for an escaped bad die
- Standards to ensure quality of substrate
- Chiplet testability may require additional die area (costs)

Interoperability

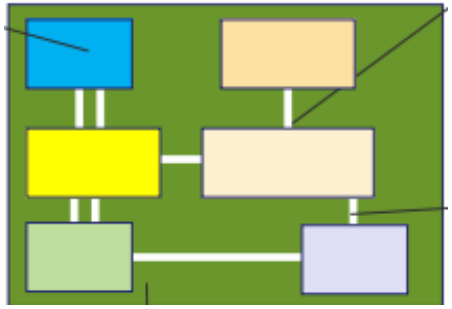
- Standardization and extension of existing test standards

Interface Best Practices

- Standard driver strength and test bumps
- Adequate design margin and die loopback

Interconnects

- Standard end to end simulation environments
- Need known substrate tests

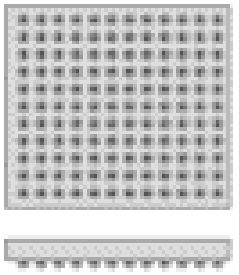


Assembling a System In Package

Chiplet Description Schema automates SiP design and build

Chiplet economy as modeled after today's silicon business will require

- Standardized design models to ensure operability in EDA workflows
- Standardized design and integration workflows for SiPs
- Integration to build SiPs in the context of multi-chiplet modules for 2.5D stacked, and 3D Integrated circuits
- Electronically readable descriptions must include following information:
  - Thermal
  - Physical/Mechanical
  - Behavioral
  - Power, Power/Signal Integrity
  - Electrical, Test
  - Security information



```
schema.xsd
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```
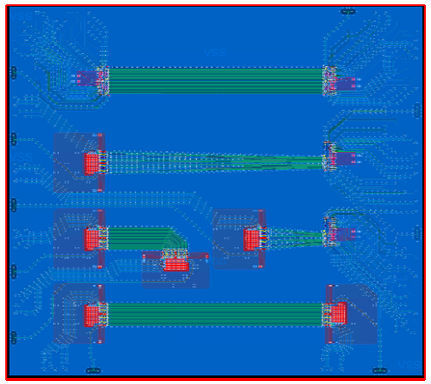

Standardized Chiplet test bench for interoperability and 3rd party validation

Accelerating the Emerging Market

- Interop, testing and validation facilitates deployments in commercial products
- An open test platform benefits everyone
- Common API for Chiplet diagnostics reduces friction
- Standardized Chiplet signal and power integrity testing
- Test across different interconnect structures and data rates
- Open source test software reduces effort

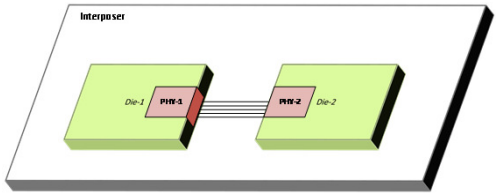


Chiplet Interconnect Test Patterns

Standardized interconnect comparison benchmark enable informed choice

Provide Community Developed and Common Criteria
Precise definition of all criteria extreme importance

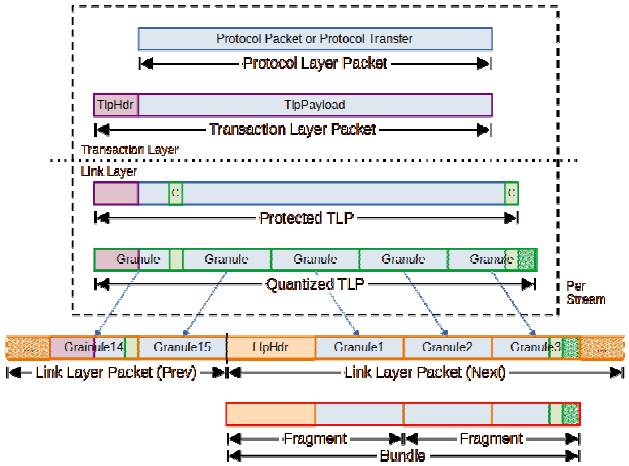
- Piece cost per Unit
  - Examines manufacturing cost implications imposed by interconnect and substrate area requirements
- Operating Cost
  - Covers power vs performance at specific throughput
- Design Impact
  - Measures routing flexibility, ease of process node diversity and complexity of IP block integration and test
- Product Integration
  - Evaluates die interface test, assembly and port complexity
- Packaging Cost
  - Counts manufacturing costs for different substrates (2D, 2.XD and 3D integration)



Standard logical interconnects allow physical interconnect interchangeability

Community Derived Link Layer (Open Spec)

- **Simplicity:** focus on die disaggregation; eliminate complexities of CDR, CRC/retry, etc.
- **Low Latency:** enable aggressive implementation techniques; use FEC to eliminate serialization overhead of CRC
- **Scalability:** support different lane data rates and slices
- **Portability:** interfaces can be built with different implementation methodologies and process nodes
- **Extensibility:** create a modular framework (interface profiles):
  - Addition of new features
  - Allow customization
  - Enable interoperability across interconnects



Physical Interconnect (BoW) is natural choice to extend AXI for Chiplets

- Specification Optimized for Maximum Applicability
  - Designer can select operating point that matches use case
  - Minimalist approach to required features
  - Single logical unit (16 lane slice) applies to all package options
  - No direct requirements on channel loss or crosstalk, conformance based upon error rates
  - Specifies signal ordering at the Chiplet edge, rather than explicit bump maps
- Key Attributes for Economies of Scale
  - Cost and energy-efficient (0.25 -0.5pJ/bit)
  - High-performance (2-16Gb/s/line) across wide range of process nodes (65nm – 5nm)
  - Use cases (25mm reach, <1e-15 BER)
  - BoW-384 (24Gb/s/line) and BoW-512 (32Gb/s/line) under construction

BoW block diagram